

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Kevin Raymond Driscoll

Serial No.: Concurrently Herewith

Filed: November 18, 2003

Docket No.: 13358.0010USC1

Title: Simple Fault Tolerance For Memory

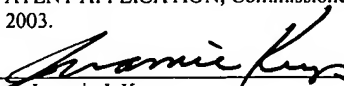
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By:



Name: Jeramie J. Keys

PRELIMINARY AMENDMENT

Mail Stop PATENT APPLICATION

Commissioner for patents

P.O. Box 1450

Alexandria, VA 22313-1450

Dear Sir:

Prior to the initial examination, please enter the following amendments to the claims starting on page 2. Note that claims 1 and 14 as amended below set forth the same recitations as claims 8 and 21 as originally filed in the parent application, which were previously rejected under 35 U.S.C. 102(b) as being anticipated by Douceur, U.S. Pat. No. 5,838,893. Applicants assert that this rejection should not be reinstated against claims 1 and 14 as amended below as the '893 patent fails to teach that the remapping value is only combined with bad address values but instead describes applying the remapping value to all address values. This is evident from the specification and FIG. 5 of the '893 patent which shows page 0 being remapped to page 10 even though the bad page is page 5, which is remapped to page 15.